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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,116	03/30/2001	Michael N. Derr	219.39308X00	3264

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EXAMINER	
PRIETO, BEATRIZ	

ART UNIT	PAPER NUMBER
2142	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,116	DERR, MICHAEL N.	
	Examiner	Art Unit	
	Prieto Beatriz	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3 and 5-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 5-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Amendment filed 05/20/05, claims 2-3, 6-7 and 9-11 have been amended, claims 1 and 4 have been canceled, claims 20-21 have been added, thereby, claims 2-3, 5-21 remain pending.

2. Regarding claims 14-15, 18 and 19 recite the acronym IDE, it is respectfully suggested to spell-out this acronym where it initially appears. Correction is required.

Claim Rejection under 103

3. Quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action may be found in previous office action.

4. Claims 2-3, 5-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over BAKER (US 5,996,032) in view of RUNALDUE et. al. (US 5,999,441) (referred to as Runaldue hereafter).

Regarding claim 12, Baker teaches a computer (Fig. 1) comprising:

a processor subsystem supported by bus 24 & 26 (Fig. 1);

a device (18), which transfers data to or from, said processor subsystem (col 10/lines 54-57, and col 5/lines 35-39) and a device (14), which transfer data to/from said processor (col 7/lines 38-48, col 6/lines 3-14 and col 21/lines 50-56);

a controller (20) adapted to control the transfer of data between said device and said subsystem (col 5/lines 20-45); and

writing in a register only the bits at the bit locations in the register for with the enable bit in the corresponding location in the bit enable field is set with the corresponding location in the data field (abstract, col 10/lines 60-col 11/line 20, col 16/lines 44-52); however does not explicitly teach where the number of enable bits in the bit enable field is the same as the number of bits in the register where the data is to be written.

Runaldue teaches writing individual bits of data to a "register" memory (10) (col 1/lines 14-17, 60-64 and col 2/lines 51-56), said method comprising:

receiving bits of input data in a data field (DATA [0:7]) to be stored in said register, the register composed of memory cells (12) arranged in eight columns [0:7] (14), thereby the number of bits in said input data field being equal to the number of bits in the register and bit locations in the data field corresponding respectively to "bit locations" addresses in the register (Fig. 1, and col 3/lines 30-57);

receiving enable bits in a bit enable field (BIT_EN) from logic (18), the number of enable bits in the bit enable field being equal to the number of bits in the register and "bit locations" addresses in the bit enable field corresponding respectively to "bit locations" addresses in the register (col 3/lines 65-col 4/line 5, col 5/lines 28-29 and col 1/lines 19-41), and

overwriting only the bits at the bit locations of the register according to the write enable bits in the write enable field (WRTDAT) for which the enable bit in the corresponding location in the bit enable field is set with the bit of input data in the corresponding location in the data field (col 2/lines 7-12, 20-32).

It would have been obvious to one ordinary skilled in the art at the time the invention was made given the suggestion of Runaldue for applying the his teachings to application using random access memory for storing data having multiple configuration lengths, the applicability to Baker environment including PC cards, i.e. memory cards, e.g., a SRAM (Static Random Access Memory) card, ROM (Read Only Memory) card, using IEEE 1394 standard communication (and suggesting the use of other different types of communication buses), typically used for communicating via telephone lines, a LAN card for connecting PCs via LAN, a SCSI (Small Computer System Interface) card for connecting to a SCSI apparatus, a sound card for playing music or producing sound effects by a PC, an ISDN (Integrated Services Digital Network) card for connecting to ISDN lines, and a Video Capture card for capturing a video signal. Motivation to combine would be modify data, such as individual bits of an addressed word within a single clock, reducing latency.

Regarding claim 13, an interconnecting device/means "bridge" (20 or 34) between the processor subsystem and at least said device, the controller being included in the switch or multiplexing function device (Baker: col 30/lines 22-54 Fig. 26a).

Regarding claim 14, wherein the device comprises an storage device (Baker: 22) and the bridge comprises an "I/O controller hub" (ICH), which controls an IDE data, transfer between the processor subsystem and the IDE storage device (Baker: col 30/lines 22-54 Fig. 26a).

Regarding claim 15, this claim is substantially the same as claim 10, same rationale of rejection is applicable.

Regarding claim 16, this claim comprises the software program stored in a tangible medium, said program, when executed, causing a computer to execute a method of claim 1, discussed above, same rationale of rejection is applicable.

Regarding claim 17, wherein said software program comprises a driver in the operating system software executed by a processor subsystem in the computer (Baker: host processor 44).

Regarding claims 18-19, this claim is substantially the same as combined limitations claims 1-3, and 9-10, same rationale of rejection is applicable

Regarding claims 2-3, wherein the register is a "control" register for a data transfer operation (BAKER: 58 on Fig. 2 control and status registers), including transfers data to or from an storage device (Baker: data transfer to or from said processor subsystem col 10/lines 54-57, and col 5/lines 35-39) and data transfer to/from said processor col 7/lines 38-48, col 6/lines 3-14 and col 21/lines 50-56);

Regarding claim 5, wherein the control register is an "IDE DMA" status register (Baker: 76 on Fig. 2), and wherein the control register is a command register (Baker: col 17/line 66-col 18/line 50).

Regarding claims 6-8, wherein some of the bits of said register are not overwritten (Runaldue: col 2/lines 25-32), wherein the data field and the bit enable field are received in parallel (Runaldue; col 2/lines 14-25) and wherein the data field is provided at an address which is contiguous with the address for the bit enable field (Runaldue: 7-bit address signal (ADDR) [0:7] of Fig. 1, i.e. continuous).

Regarding claim 9, wherein the data transfer operation comprises an IDE data transfer between a processor subsystem and an external IDE storage device (137) (Runaldue: Fig. 2).

Regarding claim 10, wherein the processor subsystem posts an entire command sequence for setting up the IDE data transfer (Baker: col 14/lines 64-66).

Regarding claim 11, wherein the method is carried out in controller in a interconnecting device or means connected between the processor subsystem and the external IDE storage device or peripheral supporting all data transfers therein (Baker: col 6/lines 39-59).

Regarding claim 20, the combined teachings as discussed above, further teach

receiving data of a single write command wherein the received data comprises a "data" input write data field (252) comprising an arbitrary number of bits, a write strobe signal (264), and an address bit field [1:4] (266) of a register where data is to be written, and an write enable bit (258),

the outputted write command data (270) comprising: the address bit field (272) comprising a register address bit (274) and an individual bit select field (276) addresses bits (Fig. 10);

modifying or changing the register with one or more bits of the data field that are associated with the enable bits of the bits enabled field (Baker: col 16/line 32-col 17/line 10).

Regarding claim 21, where the data (270) of the single write command comprises at least two bits (Baker: 1 to 4 GPIOs to be written, col 16/lines 53-55), the write enable field (258) comprises one or more bit, and the input write data field comprises any number of bits (Baker: col 16/lines 32-46).

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prieto, B. whose telephone number is (571) 272-3902. The Examiner can normally be reached on Monday-Friday from 6:00 to 3:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, Andrew T. Caldwell can be reached at (571) 272-3868. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800/4700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system, status information for published application may be obtained from either Private or Public PAIR, for unpublished application Private PAIR only (see http://pair-direct.uspto.gov or the Electronic Business Center at 866-217-9197 (toll-free).

Any response to this action should be mailed to:
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Customer Service Window located at the Randolph Bldg.
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Faxed to the Central Fax Office:
(703) 872-9306 (old No. in service until Sept. 15, 2005),
(571) 273-8300 (New Central Fax No.)

Or Telephone:

(703) 306-5631 for TC 2100 Customer Service Office.

Beatriz Prieto
BEATRIZ PRIETO
PRIMARY EXAMINER

B. Prieto
TC 2100
Primary Examiner
July 16, 2005